REMARKS

Claims 1, 2, 4-8, 10-14, and 16-19 stands rejected under 35 USC §112, second paragraph. Claims 1, 2, 4-8, 10-14, and 16-19 stands rejected under 35 USC §102(b) as being anticipated by Pochmuller, U.S. patent 6,295,237.

Claims 1, 5, and 17 have been amended to more clearly state the invention. Reconsideration and allowance of each of the pending claims 1-2, 4-8, 10-14, and 16-19, as amended, is respectfully requested.

Reconsideration and withdrawal of the rejection of claims 1, 2, 4-8, 10-14, and 16-19 under 35 USC §112, second paragraph, is respectfully requested in view of claims 1, and 17, as amended.

Pochmuller, U.S. patent 6,295,237 discloses a semiconductor memory configuration, in particular a DRAM, in which redundant memory cells, bit lines and word lines are determined for failed memory cells, failed word lines and failed bit lines by a built-in-self-test computing unit and a special algorithm. In a test, the individual memory cell arrays are checked by driving their word lines and bit lines in order to determine defective memory cells, word lines and bit lines. The results of this test are stored in a register 12. However, it is also possible to store the results in the defective DRAM itself. Thus, by way of example, when the memory array 1 is being tested, the results can be stored in the as yet untested memory array 10. This does, however, presuppose highly redundant storage of the information. A built-in-self-test (BIST) computing unit 14 with a counter unit 15 for counting the hit values up to an upper limit then evaluates the results of the tests. The results finally being stored in the registers

12, after the conclusion of the tests and determines those redundant memory cells, bit lines and word lines which, as the spare memory cells, spare bit lines and spare word lines from the memory cell array 10, are intended to replace the defective memory cells, bit lines and word lines in the memory cell arrays 1, 2, . . . , n. The replacement of the memory cells, the bit lines and the word lines is effected, for example, via corresponding bus lines 11, which connect the individual memory cell arrays to one another.

Applicants respectfully submit that each of the pending independent claims 1 and 17, as amended, is patentable over the references of record including the cited Pochmuller, U.S. patent 6,295,237.

As amended, each of the pending independent claims 1 and 17 respectively recite features of the method and apparatus for detecting degradation in an integrated circuit that are only taught by Applicants. More specifically, as amended, the pending independent claims 1 and 17 further define the MBIST engine controlling operation of said at least one monitor element; communicating monitor bits, and deterministically stressing said predefined circuit element functions of said at least one monitor element; and identifying degradation of each of array signal, array timing, and voltage margins utilizing said at least one monitor element and that the MBIST engine reciting the step of providing or to include MBIST control circuitry and MBIST registers; using the at least one monitor element or being used with said MBIST engine to identify a degraded situation for enabling appropriate preventative action; and providing latch circuitry coupled to said MBIST engine for latching monitor bits, said latch circuitry used

to communicate with said MBIST engine. These features are not shown, nor suggested in Pochmuller or any of the references of record. Thus, each of the pending independent claims 1 and 17, as amended, is patentable over Pochmuller.

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in a prior art reference. Thus, reconsideration and withdrawal of the rejection of 35 U.S.C. § 102 is respectfully requested.

Pochmuller teaches a semiconductor memory configuration including a DRAM, in which redundant memory cells, bit lines and word lines are determined for failed memory cells, failed word lines and failed bit lines by a built-in-self-test computing unit and a special algorithm, with redundant memory cells replacing failed memory cells of the memory cell array.

Pochmuller does not show, nor remotely suggest deterministically stressing said predefined circuit element functions of said at least one monitor element; and identifying degradation of each of array signal, array timing, and voltage margins utilizing said at least one monitor element, as now expressly recited in each of the pending independent claims 1 and 17, as amended. Applicants respectfully submit that the present invention as recited by independent claims 1 and 17, as amended, is patentable over Pochmuller.

Dependent claim 5, as amended, further define that deterministically stressing said predefined circuit element functions of said at least one monitor element includes selectively controlling timing, data pattern, frequency of access, frequency of refresh, enabling, and heating of said predefined circuit elements of said at least one

monitor element. Dependent claim 5, as amended, is patentable over Pochmuller.

Dependent claims 2, 4-8, 10-14, 16, and 18-19 further define the invention depending from respective patentable claims 1 and 17. Thus, each of the dependent claims 2, 4-8, 10-14, 16, and 18-19 is patentable.

Reconsideration and allowance of each of pending claims 1-2, 4-8, 10-14, and 16-19, as amended, is respectfully requested.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-2, 4-8, 10-14, and 16-19, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

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